Printed Pages: 2 **Sub Code: NMCA215**

Paper Id: 214223 **Roll No.** | | | | | | | | | | |

MCA

(SEM II) THEORY EXAMINATION 2018-19

COMPUTER ORGANIZATION

Time: 3 Hours *Total Marks: 100*

Note: 1. Attempt all Sections. If required any missing data, then choose suitably.

SECTION A

1. Attempt all questions in brief. **2 x 10 = 20**

a. Describe the role of carry generate function in designing the fast adders.
b. Differentiate between macro operations and micro operations.
c. Define the internal organization of a computer.
d. List out various steps involved in the execution of an instruction.
e. Discuss the role of control store in micro programmed control unit.
f. What is the difference between rotate and rotate thru carry type shift instructions.
g. What are the advantages of using many registers?
h. What do you mean by stored program concept?
i. Discuss the term I/O interface.
j. How the cache memory works? Explain.

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a. Explain the algorithm for addition-subtraction of signed-magnitude numbers with the help of flowchart.
b. How the arithmetic or logic operations are performed using single bus organization of the data path inside the processor? Explain.
c. Discuss various logical and bit manipulation instructions with example.
d. What are various modes of transfer? Discuss each of them.
e. A CPU data bus has 16 lines and its address bus contains 12 lines. What is the maximum memory capacity that can be connected to the CPU? How many bytes can be stored in memory?

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

(a) Discuss single and double precision IEEE standards for floating point numbers with the help of examples.
(b) What do you mean by bus? Discuss bus and memory transfers.

4. Attempt any *one* part of the following: **10 x 1 = 10**

(a) Explain the working of the organization of hardwired control unit with the help of diagram.
(b) How many micro operations can be performed in case of n binary variables? List out various logic micro operations performed on two binary variables.

5. Attempt any *one* part of the following: 10 x 1 = 10

(a) How the expression can be evaluated using stack. Describe memory stack and register stack organization of the processor.

(b) Write down the three, two, one, and zero address instructions for the expression X:=(A+B) * (C+D)

6. Attempt any *one* part of the following: 10 x 1 = 10

(a) What is the various variety of addressing modes? Discuss register indirect and memory indirect mode of instruction with example.

(b) What do you mean by DMA? Discuss its I/O operations.

7. Attempt any *one* part of the following: 10 x 1 = 10

(a) Discuss address mapping and associate memory page table used in case of virtual memory.

(b) The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80% of memory requests are for read and the remaining 20% for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.

i. What is the average access time of the system considering only memory read cycles?

ii. What is the average access time of the system for both read and write requests?

iii. What is the hit ratio taking into consideration the write cycles?